CLAIMS

What is claimed is:

1. A method comprising:

forming a dielectric on a contact, the contact formed on a substrate;

forming an opening through the dielectric exposing the contact;

forming a programmable material within the opening, the programmable material on the contact; and

forming a conductor to the programmable material.

2. The method of claim 1, wherein dimensions of the opening expose a first contact area of the contact, the method further comprising forming at least one spacer within the opening on the contact, the spacer exposing a second contact area of the contact having dimensions less than the first contact area, wherein the programmable material is on the second contact area of the contact.

3. The method of claim 1, further comprising:

forming a barrier material between the programmable material and the conductor.4. The method of claim 1, wherein the contact transmits to a signal line, the method further comprising forming an isolation device between the contact and the signal line.

5. The method of claim 2, wherein forming the at least one spacer comprises:

conformally forming at least one spacer on a surface of the dielectric and within the opening; and

anisotropically etching the at least one spacer from the surface of the dielectric.

6. The method of claim 5, wherein the anisotropically etching comprises anisotropically etching with an agent that is selective for the spacer.

7. An apparatus comprising:

a contact on a substrate;

a dielectric on the contact, the dielectric having an opening exposing the contact;

a programmable material formed within the opening, the programmable material on the contact; and

a conductor in contact with the programmable material.

8. The apparatus of claim 7, wherein dimensions of the opening expose a first contact area of the contact, the apparatus further comprising a spacer within the opening on the contact, the spacer exposing a second contact area of the contact having dimensions less than the first contact area, wherein the programmable material is on the second contact area of the contact.

9. The apparatus of claim 7, further comprising:

a barrier material between the programmable material and the conductor.

10. The apparatus of claim 7, further comprising:

a signal line in contact with the contact; and

an isolation device between the contact and the signal line.

11. The apparatus of claim 7, wherein the at least one spacer comprises a conformally formed spacer on the dielectric, and wherein the at least one spacer comprises an anisotropically etched spacer from the dielectric.

12. The apparatus of claim 7, wherein the programmable material comprises a chalcogenide memory element.

13. A system comprising:

a microprocessor;

an input/output (I/O) port; and

a memory including a contact on a substrate, a dielectric on the contact having an opening exposing the contact, a programmable material formed within the opening and on the contact, and a conductor in contact with the programmable material; and

wherein the microprocessor, the I/O port, and the memory are connected by a data bus, an address bus and a control bus.

14. The system of claim 13, wherein dimensions of the opening expose a first contact area of the contact, the system further comprising a spacer within the opening on the contact, the spacer exposing a second contact area of the contact having dimensions less than the first contact area, wherein the programmable material is on the second contact area of the contact.

15. The system of claim 13, further comprising:

a barrier material between the programmable material and the conductor.

16. The system of claim 13, further comprising:

a signal line in contact with the contact; and

an isolation device between the contact and the signal line.

17. The system of claim 14, wherein the at least one spacer comprises a conformally formed spacer on the dielectric, and wherein the at least one spacer comprises an anisotropically etched spacer from the dielectric.

18. The system of claim 13, wherein the programmable material comprises a chalcogenide memory element.